Publishable summary

POLYSYS

*Direct 100G connectivity with optoelectronic **POLY**mer-InP integration for data center **SYS**tems*

Grant Agreement No. 258846

Project duration: 36 months

Project website: http://www.ict-polysys.eu

Overview of the project

New broadband applications continue to emerge, increasing the required bandwidth in every part of the network. The amount of information that is exchanged today is creating real pressures in modern data-centers. The incorporation of thousands of servers has created the necessity to transfer massive amounts of data between racks, boards and modules quickly, efficiently and at low cost. Connectivity is thus a key factor, and it is today well understood that electrical cables and low cost commodity hardware cannot accommodate this explosion of required bandwidth. The "infiltration" of photonics in data-centers is already evident and optical interconnects tend to replace electrical cables over shorter and shorter lengths: starting from rack-to-rack connectivity, active optical cables are available in a rapidly growing market. Moving to shorter distances, optical interconnects will ultimately penetrate into board-level to provide chip-to-chip connectivity. To reach Tb/s capacities an integration technology capable of serial ultra-high speed modulation is believed today to be the missing piece. POLYSYS is aiming to provide the disruptive solution to realize for the first time serial 100 Gb/s direct connectivity in datacom and telecom systems. POLYSYS is developing photonic and electronic components operating at 100 Gb/s based on electro-optic polymer modulators, InP photodiodes and InP electronics. The technical objectives of POLYSYS will be achieved through the use of hybrid integration for the assembly of the different components and the use of advanced packaging methodologies for the final packaging of the modules and systems. More specifically, the modules that are targeted include a 100 Gb/s transmitter (Module 1), a 100 Gb/s receiver (Module 2), an arrayed 2x100 Gb/s transmitter (Module 3), an arrayed 4x100 Gb/s receiver (Module 4), a 100 Gb/s transmitter with wavelength tunability (Module 5) and a 100 Gb/s receiver with clock-recovery functionality (Module 6). The six modules will be combined for developing three systems that address discrete applications: on board (chip-to-chip) optical interconnects (System 1), rack-to-rack interconnects based on active optical cables (System 2), and 100 Gb/s transceivers for 100 GbE applications (System 3).

Work performed and results achieved

The main technical achievements for Year 2 of the Project are summarized below per work-package.

Work Package 2: System design and methodology for integration and packaging processes

Activities within WP2 relate to the definition of the system-level specifications of the POLYSYS modules and systems, the selection of the components that are integrated inside each module, the definition of the general methodologies for the interfacing of components and the packaging of modules, the system-level simulations of the devices and the experimental characterization of testing structures, precursor units and early devices in order to provide valuable feedback for the continuation of the design and development activities in the other work-packages. In Year 3, the main activities related to the redesign of the system for the chip-to-chip interconnect (System 1), the redesign of the 2x100 Gb/s transmitter (Module 3), the update on the system-level specifications, the update of the simulation setups and the experimental characterization of polymer periodic filters and polymer Bragg-grating-based laser structures with

wavelength tunability over 17 nm. Preparation of the detailed layouts of all modules has progressed and will be completed in Year 3.

Work package 3: Monolithic polymer and InP-to-polymer integration

WP3 targets at the design and the fabrication of the passive structures on the polymer platform (bent waveguides, MMI couplers, Bragg-gratings), the fabrication of the modulators on the same electro-optic substrate, the development of the butt-coupling technique for the integration of the InP components to the polymer platform, and the final preparation and delivery of the optical sub-assemblies that are needed for the POLYSYS transmitters (Module 1, Module 3 and Module 5) and the optical integrated interconnect (System 1). In Year 2, the polymer structures that were fabricated during the first fabrication run were tested and confirmed the feasibility of the total of the relevant concepts that POLYSYS project has been based on: the feasibility for monolithic integration on the electro-optic platform of Bragg-gratings with sufficient reflectivity, the feasibility for external cavity tunable lasers using the polymer Bragg-grating as the semi-transparent mirror of the cavity, the feasibility of monolithic integration of 1:2 and 1:4 multi-mode interference (MMI) couplers with low insertion loss (<1 dB), and the feasibility of butt-coupling InP DFB lasers, gain media and waveguide-integrated pin-photodetectors to the polymer waveguides for the implementation of complex photonic integrated circuits (PICs). In Year 2, the optical-subassemblies of the 100 Gb/s transmitter and the integrated optical interconnect were prepared and delivered for further integration with the InP electronics. Optimization of all polymer structure designs was made in view of the second fabrication run, which is expected to be completed in the beginning of Year 3.

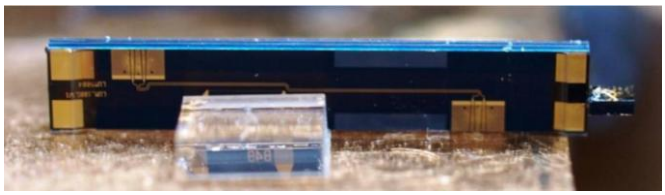

Figure 1: Optical assembly of the 100 Gb/s transmitter consisting of the DFB laser and the 100 Gb/s polymer modulator board. The polymer modulator was based on the relevant technology of GigOptix. The hybrid integration of the polymers with the InP actives was designed, optimized and realized by the polymer group of HHI.

Work package 4: InP photonics and electronics

WP4 activities are devoted to the design and development of the InP photonic and electronic components. The photonic components include the arrayed (4x100 Gb/s) pin-photodiodes and the arrayed (4x100 Gb/s) pin-photodiodes followed by travelling wave amplifiers (pinTWAs). The electronic components on the other hand include the MUX-DRV circuit that implements the 2:1 multiplexing and the amplification functionalities, the 1:2 DEMUX circuit (single- and twin-DEMUX circuits) and the clock-and-data recovery (CDR) circuit, all of them being capable of operating at 100 Gb/s line rate.

In Year 2, the receiver group of HHI completed the fabrication and the on-wafer characterization of arrayed pin-photodetectors confirming high-conversion gain and 100 GHz bandwidth properties. The design of the pinTWA arrays was completed, and first photodiode wafers were successfully employed for the overgrowth of the high electron mobility transistors (HEMTs) for the TWA part of the devices. The fabrication of the pinTWA arrays will be completed in the last year of the project. On the other hand, III-V Lab completed the development and characterization of two versions of MUX-DRV circuits and made them available for the assembly of the 100 Gb/s transmitter and the integrated optical interconnect (System 1). Both versions are capable of 100 Gb/s operation providing differential output of 2x2V (version 1) and 2x3V (version 2) amplitude. Different versions of single DEMUX circuits were also characterized confirming their 100 Gb/s capabilities, and the twin-DEMUX circuit was designed and fabricated. Its characterization will follow in

Year 3. Finally the main blocks of the CDR circuit were designed and entered the fabrication stage. Experimental assessment of this circuit will be made in the final year.

Work package 5: Photonic packaging and system integration

Activities within WP5 are devoted to the integration of the individual components and the final packaging of the POLYSYS modules/systems. In Year 2 the packaging approaches concerning thermal management issues, design of high-speed electrical interconnects, design of electrical transitions, type of output connectors and optimization of fiber pigtails were optimized and finalized. TEO proceeded with the assembly and the packaging of the first POLYSYS module (100 Gb/s transmitter) using this methodology. The exceptionally high performance of the device, as revealed through system experiments, confirmed the effectiveness of the packaging methodology and approach. The assembly of the next module/system (100 Gb/s integrated interconnect) started and is expected to have been completed in the beginning of Year 3. Numerical simulations and detailed designs have also been realized by TEO and HHI regarding the packaging of the 2x100 Gb/s transmitter and the 4x100 Gb/s pinDEMUX and pinTWA-DEMUX receivers.

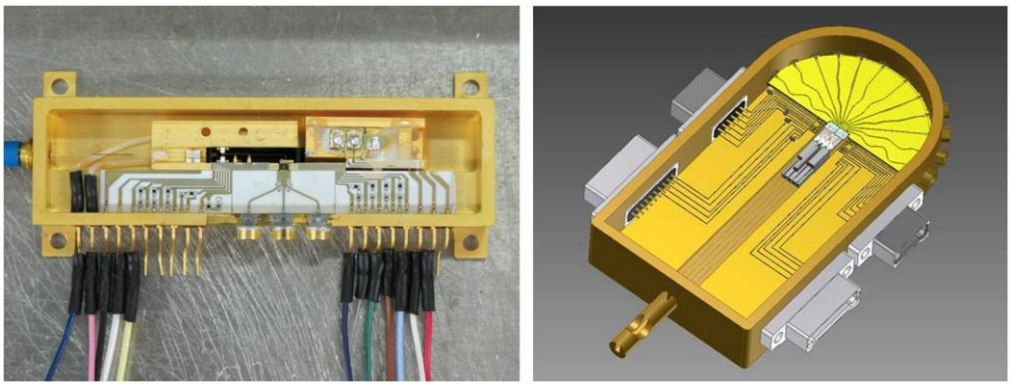

Figure 2: (Left) Photograph of the 100 Gb/s transmitter that was successfully assembled and packaged by TEO in Year 2 of POLYSYS. Inside the package the components that have been integrated include a DFB laser, a polymer modulator, and a MUX-DRV circuit. (Right) Design of the package that will be used for the packaging of the 4x100 Gb/s pin-DEMUX and pinTWA-DEMUX receivers in Year 3 of POLYSYS. The design was made by HHI.

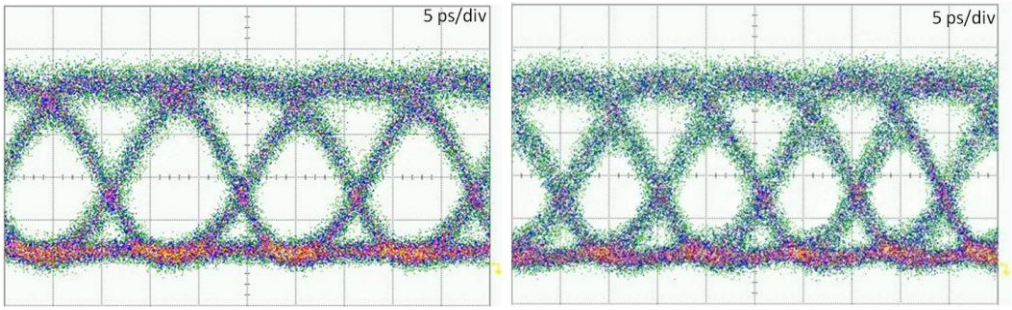

Figure 3: Eye-diagrams of the optical signal at the output of POLYSYS transmitter at 80 Gb/s (left) and 100 Gb/s (right). BER measurements revealed error-free operation both at 80 and 100 Gb/s and confirmed the advancement of POLYSYS technology with respect to the state-of-the-art in high-speed optical transmitters. The module was evaluated in the system testbed of ICCS/NTUA.

Work package 6: System testing and evaluation

The main objective of WP6 is the development of the system testbed and the evaluation of the performance of POLYSYS modules and systems. In Year 2, ICCS/NTUA designed and developed a 100 Gb/s system testbed with possibility to scale up to 4x100 Gb/s. The main evaluation parameters were identified and specific testing protocols were defined for the assessment of the POLYSYS transmitters, receivers and systems in datacom and telecom environments. ICCS/NTUA proceeded with the testing of the 100 Gb/s transmitter. Clearly open eye-diagrams with high extinction ratio (> 13 dB) and error free performance

were confirmed in the 80-100 Gb/s range using different setups for the demultiplexing and the final bit-error-rate (BER) measurements. The combination of these results confirms the effectiveness of the design of the individual components and the effectiveness of the packaging methodology, and constitutes a clear advancement with respect to the state-of-the-art in high-speed transmitters, which has been achieved by POLYSYS achieved already in the second year of the project. System-level evaluation activities will continue in Year 3 with transmission experiments and the evaluation of the next modules/systems.

Work package 7: Applicability, techno-economical assessment and integration standardization

Main objectives of WP7 include the exploitation and dissemination of the project results by the partners. In Year 2, the consortium prepared an applicability and techno-economic analysis for the POLYSYS technology identifying application areas, where this technology may have significant advantages in terms of cost, energy efficiency, simplicity and performance over alternative approaches. Partners updated their exploitation plans and achieved to increase significantly the visibility of the project through 13 publications, participation at OFC 2012 and ECOC 2012 exhibitions, press-releases and events towards the general public. Highlight in the dissemination activities in Year 2 has been the achievement of an ECOC 2012 post-deadline publication on the assembly and the experimental characterization of the 100 Gb/s integrated transmitter.

Expected results at the end of the project

As described above, the targeted modules include single and arrayed 100 Gb/s transmitters and receivers that will be combined in three systems to address three discrete application areas: chip-to-chip optical interconnects, rack-to-rack interconnects and 100 GbE metro applications.

Expected impact

POLYSYS exploitation plan relies on the fact that serial technologies have always overtaken more complex parallel approaches. POLYSYS will develop photonic and electronic components operating directly at 100 Gb/s, and using arrayed versions of these components will demonstrate 400 Gb/s connectivity. This is expected to have a disruptive effect in the current development curve of 100G systems that rely on 10x10 Gb/s or 4x25 Gb/s components (either for datacom or telecom applications). The achievement of the challenging objectives of POLYSYS will bring Europe at the forefront of 100G photonic/electronic component market. Through the exploitation of the project results, POLYSYS partners will be in the position to offer a technology solution with unmatched performance (direct 100 Gb/s connectivity, scalability to Terabit per second capacities) and lower cost compared to competing technological approaches.

Contractors involved

	INSTITUTE OF COMM. & COMPUTER SYSTEMS/ NATIONAL TECHNICAL UNIVERSITY OF ATHENS	GR
Fraunhofer Heinrich Hertz Institute	FRAUNHOFER HEINRICH HERTZ INSTITUT	GE
III-V lab ALCATEL-THALES	ALCATEL-THALES III-V LAB	FR
GIGOPTIX	GIGOPTIX-HELIX AG	CH
TELEOPTIX	LINKRA-TELEOPTIX	IT

Coordinator contact details

Prof. Hercules Avramopoulos

National Technical University of Athens
9 Iroon Polytechniou Street, 15773, Athens, GREECE

Tel: +30-210 772 2076
Fax: +30-210 772 2077

e-mail: hav@mail.ntua.gr