POLYSYS

*Direct 100G connectivity with optoelectronic **POLY**mer-InP integration for data center **SYS**tems*

Grant Agreement No. 258846

Project duration: 36 months

Project website: http://www.ict-polysys.eu

Overview of the project

New broadband applications continue to emerge, increasing the required bandwidth in every part of the network. The amount of information that is exchanged today is creating real pressures in modern data centers. The incorporation of thousands of servers has created the necessity to transfer massive amounts of data between racks, boards and modules quickly, efficiently and at low cost. Connectivity is thus a key factor and it is today well understood that electrical cables and low cost commodity hardware cannot accommodate this bandwidth explosion. The "infiltration" of photonics in data centers is already evident and optical interconnects tend to replace electrical cables over shorter and shorter lengths.

Starting from rack-to-rack connectivity, active optical cabling products are available in a rapidly growing market. Moving to shorter distances, optical interconnects will ultimately penetrate into board-level and chip-level connectivity. To reach Tb/s capacities an integration technology capable of serial ultra-high speed modulation is believed today to be the missing piece.

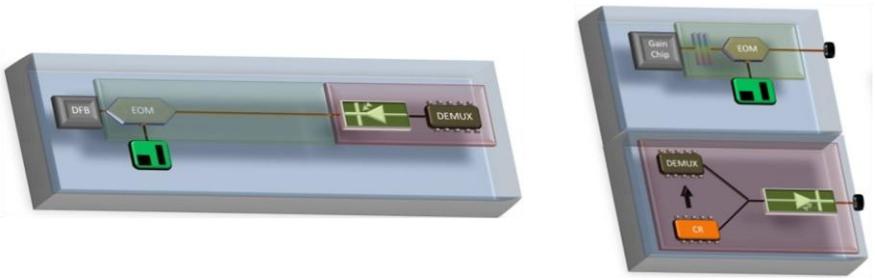

Figure 1: *Artistic layout of POLYSYS system for 100 Gb/s chip-to-chip interconnect (left), and 100 Gb/s optical transceiver for 100 GbE telecom applications (right).*

POLYSYS aims to provide this disruptive solution to realize for the first time serial 100 Gb/s direct connectivity in datacom as well as in telecom systems. POLYSYS is developing photonic and electronic components operating directly at 100 Gb/s based on electro-optic polymer modulators, InP photodiodes and InP electronics. The technical objectives of POLYSYS are to be achieved through the use of hybrid integration techniques for the assembly of the different piece-parts and the use of advanced packaging designs and methodologies for the final provision of functional modules and systems. More specifically, the modules that are targeted involve a 100 Gb/s transmitter (Module 1), a 100 Gb/s receiver (Module 2), an arrayed 400 Gb/s transmitter (Module 3), an arrayed 400 Gb/s receiver (Module 4), a 100 Gb/s tunable (in wavelength) transmitter (Module 5) and a 100 Gb/s receiver with clock-recovery functionality (Module 6). The six modules are to be combined in order to develop three systems that address three discrete application areas: chip-to-chip optical interconnections, direct connectivity between server racks, and 100 Gb/s transceivers for 100 GbE applications. The artistic layouts of the targeted systems for the chip-to-chip optical interconnect and the 100 GbE applications are depicted in Figure 1.

Work performed and results achieved

The main technical achievements for the Year 1 of the Project are summarized below per work package.

Work Package 2: System design and methodology for integration and packaging processes

Activities within WP2 enable the exchange of technical information among partners, define the system level specifications of the POLYSYS components, identify the critical interfaces between the individual components and investigate their compatibility, build the device models for the system-level simulations of POLYSYS systems, define the methodology of the integration/packaging techniques and perform preliminary evaluation of test structures in order to refine the specifications of the components.

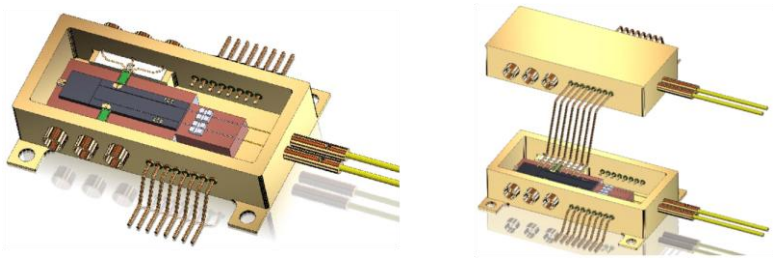

Figure 2: *Layout of the 2x100 Gb/s transmitter (left), and of the arrangement for the twin 2x100 Gb/s module (right).*

Within the first period of POLYSYS, the consortium partners agreed on the definition and the general system specs of the six POLYSYS modules and the three POLYSYS systems. The main interfaces were defined and the compatibility of the components was checked. It was also decided to change the structure of the 400 Gb/s transmitter so as not to consist of a 4x100 Gb/s but rather of a twin 2x100 Gb/s module. Furthermore system level models were successfully developed and simulations were conducted. Finally, first experiments with precursor receiver units were conducted and experimental characterization of preliminary polymer chips took place.

Work package 3: Monolithic polymer and InP-to-polymer integration

WP3 targets at the design and the fabrication of the passive structures on the polymer platform (bent waveguides, MMI couplers, Bragg-gratings), the fabrication of the modulators on the same electro-optic substrate, the development of the butt-coupling technique for the integration of the III-V elements to the polymer platform, and the final delivery of the optical transmitter subassemblies.

In Period 1, bent waveguides, 1x2 and 1x4 MMI couplers and Bragg-gratings were designed using different approaches in the case of Bragg-gratings. Variation ranges were identified and multiple designs were included in the first mask-set. Simulation and experimental studies were conducted in order to calculate the theoretical limits and the actual achievable values for the coupling of light between the DFB and the polymer waveguides, as well as between the polymer waveguides and the InP receiver waveguides. The feasibility for the butt-coupling approach was confirmed. The first fabrication round was completed. A variety of structures (bent waveguides, MMI couplers and Bragg gratings were fabricated and made available to the project partners for characterization.

Work package 4: InP photonics and electronics

Within WP4, the InP photonic and high-speed electronic components are being designed and developed. The general objectives include the design and fabrication of arrayed photodetectors and photoreceivers, and the design and fabrication of various electronic components (2:1 MUX,

driver, 1:2 DEMUX, clock recovery). To succeed in the fabrication of ultra-high speed electronics new InP-DHBT processes are also developed.

Within Period 1, two diode types were designed. The mask set was designed and developed. Fabrication of a pair of wafers has started and is expected to be completed in the first months of Period 2. Extensive simulation studies were conducted and different types of TWA were considered. Numerical simulations showed that excellent performance can be reached and mask-set is now ready to be designed. Preliminary floorplan studies were completed. As far as the InP-DHBT fabrication process is concerned, the regular SHARC process of ATL has been made optimized in order to improve the thermal characteristics of the bipolar transistors. A new process (SAND process) that enables higher voltage swing was also developed. Finally, the basic MUX+DRV and DEMUX circuits that will be used in the transmitter and receiver modules of POLYSYS were developed and successfully tested at 50 and 100 Gb/s operation.

Work package 5: Photonic packaging and system integration

Activities within WP5 are devoted to the integration of the individual piece-parts and the final packaging of the six POLYSYS modules. The partners involved with these activities will gather the optical subassemblies and the electronic parts and will be assembling them inside well-designed packages. The packaged modules will be further forwarded for system-level testing.

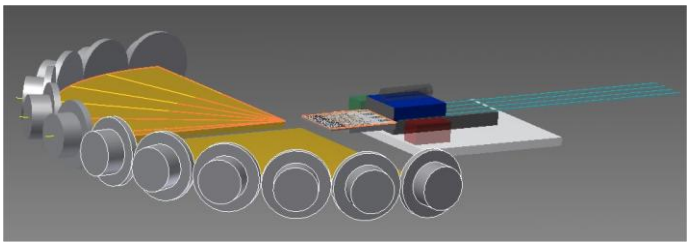

Figure 3: *3-D sketch of chip arrangement, optical coupling and network to output connectors of the planned 4x100 Gb/s photoreceiver module with DEMUX functionality (prepared by HHI).*

Within the first period, the general rules and the steps for the general packaging procedures were defined. Partners relied on this methodology and elaborated on the specific packages that will be used for the first 100 Gb/s transmitter module and the 4x100 Gb/s receiver.

Work package 6: System testing and evaluation

The main objective of WP6 is the development of the necessary system testbeds and the evaluation of the system-level performance of the POLYSYS devices, when these devices will be made available from the WP5.

Preliminary work was conducted with respect to the design and the preparation of the testbed. Within the first year of POLYSYS, the design of the 100 Gb/s testbed for the testing of the POLYSYS devices was finalized, and the required equipment and individual components were gathered and assembled. Rules and plans for extending the testbed in the 2x or 4x cases were defined.

Work package 7: Applicability, techno-economical assessment and integration standardization

The main objectives of WP7 are dissemination and exploitation of project outcomes through interactions with industry, academia, and the scientific community, and planning for exploitation of POLYSYS technology in commercial applications. Protection of intellectual property generated within POLYSYS is also important for the subsequent commercial exploitation of the project results.

During the first period of POLYSYS, the consortium members achieved four publications (two journal and two conference publications). The concepts and the first results of POLYSYS were also disseminated through booths at the exhibitions of OFC 2011 and ECOC 2011. Finally, the scientific/technical roads to follow within POLYSYS were presented during the Photonics concertation meeting that was organized by EC in October 2010 in Brussels.

Expected results at the end of the project

As already mentioned, the targeted modules include a 100 Gb/s transmitter, a 100 Gb/s receiver, an arrayed 400 Gb/s transmitter, an arrayed 400 Gb/s receiver, a 100 Gb/s tunable (in wavelength) transmitter and a 100 Gb/s receiver with clock-recovery functionality. The six modules will be combined in three systems that address three discrete application areas: chip-to-chip optical interconnections, direct connectivity between server racks, and 100 Gb/s transceivers for 100 GbE applications.

Expected impact

POLYSYS exploitation plan relies on the fact that serial technologies have always overtaken more complex parallel approaches. POLYSYS will develop photonic and electronic components operating directly at 100 Gb/s, and using arrayed components will demonstrate 400 Gb/s. This is expected to have a disruptive effect in the current development curve of 100G systems that rely on 10x10 Gb/s and 4x25 Gb/s components. The achievement of POLYSYS challenging objectives will bring Europe in the forefront of 100G photonic/electronic component market. Through the exploitation of project results, POLYSYS consortium members will be in a position to offer a technology solution with unmatched performance and cost: direct 100 Gb/s transmission bandwidth, scalability to terabit capacities, and at a lower cost compared to competing technological approaches. Application of POLYSYS technology to datacom and high-speed interconnects is envisaged through the commercialization of high-speed 100 Gb/s links based on the integrated components developed in the project: it will be pursued that 100 Gb/s high-speed modulator arrays with InP drivers and high-speed InP receivers will be put on the market shortly after the end of the project.

Contractors involved

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